Applicant respectfully submits that this response is timely filed. Due to the above actions, claims 6, 26-28, 48, 49, 63 and 74 have been canceled and claims 1-3 and 8 have been amended. Accordingly, claims 1-3, 8, 11-14, 16-19, 28, 32-34, 38-43, 52, 53, 58-60, 65, 71-73 and 75 are currently pending in the present application and, for the reasons set forth below, are believed to be in condition for allowance.

Initially, the Office Action rejects claims 6, 27, 28 and 74 under 35 U.S.C. §102(b) as being anticipated by ***Matsueda*** (U.S. Patent 5,173,792) and claim 26 under 35 U.S.C. §103(a) as being unpatentable over ***Matsueda***. Claims 6, 26-28 and 74 have been canceled, thereby rendering these rejections moot.

Claims 1-3, 8, 11-14, 16-19, 32-34, 38-43, 48, 49, 52, 53, 58-60, 63, 65, 71-73 and 75 are rejected under 35 U.S.C. §103(a) as being unpatentable over ***Takemura*** (U.S. Patent 5,581,092) in view of ***Matsueda***. Applicants respectfully traverse this ground for rejection and reconsideration of the pending claims is respectfully requested for the reasons solicited below.

The claimed invention is directed to an active matrix type display device. In particular, the claimed invention is directed to an active matrix type display device including at least two transistors provided on an insulating surface in a driver circuit of the active matrix type display device, wherein channel-forming regions of the at least two transistors are separately provided in at least two separate islands, as presently recited at least in independent claim 1 and illustrated in Figure 3 of the present invention.

As the Examiner well knows, three criteria must be met to establish a *prima facie* case of obviousness. *M.P.E.P.* §2143. First, there must be some teaching, suggestion, or motivation to combine or modify the teachings of the prior art to produce the claimed invention, found either in the references themselves or in the knowledge generally available to a skilled artisan. *In re Fine*, 837 F.2d 1071, 5 USPQ.2d 1596 (Fed. Cir. 1988). Second, there must be a reasonable expectation of success. *In re Rhinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976). Third, the prior art must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

In the Office Action, the Examiner contends that it would have been obvious to incorporate the parallel-connected TFTs disclosed in ***Matsueda*** into the peripheral driver circuit of ***Takemura '792*** so as to improve the reliability of the display device. In response thereto, Applicants' respectfully contend that the claimed invention yields unexpectedly improved properties which obviate problems in the related art which are not recognized in the

teachings of either ***Takemura '792*** or ***Matsueda***. For instance, in order to construct an integrated active matrix type display device, it is desirable to form not only the pixel region but also the peripheral circuitry on a single substrate. In such cases, the TFTs which are arranged on the peripheral circuitry should have the ability to handle large currents in order to drive the many thousands pixel electrodes. However, operating at such large currents produces excess heat and degradation of characteristics in the active matrix type display device. Accordingly, a buffer amplifier (i.e., a power conversion circuit which has a low output impedance) composed of TFTs in the peripheral circuitry is provided to handle the large currents. In order to construct a TFT which can be used in a buffer amplifier, however, it is necessary for the channel-forming region of the TFT to have a width of several tens of micrometers or more.

Accordingly, in order to obviate the aforementioned problems in the related art, Applicants' have provided an active matrix-type display device including, *inter alia*, at least two transistors provided on an insulating surface in a buffer circuit of a driver circuit, wherein channel-forming regions of the at least two transistors are separately provided in at least two separate islands respectively. Applicants' submit that certain benefits are derived from such a construction which are unobviously advantageous over the related art. For example, the active matrix-type display device of the claimed invention has a high voltage resistance and performs at high speeds which do not produce degradation or variation of characteristics. Applicants' further submit that ***Matsueda*** is not concerned with the problems obviated by the claimed invention, such as low voltage resistance, heat generation, and degradation of characteristics as a result of high speed operations. In fact, ***Matsueda*** merely discloses pixel transistors of an electro-optical display, and is silent concerning the use of a driver circuit. ***Matsueda's*** lack of recognition of the problems solved by the Applicants' is indicia of the nonobviousness of the claimed invention, and thus, the combined teachings of ***Takemura*** and ***Matsueda*** are insufficient to motivate one skilled in the art to combine them in order render the claimed invention obvious. Accordingly, Applicants' respectfully request that the §103(a) rejection of the pending claims be reconsidered and withdrawn in view thereof.

Accordingly, Applicant submits that claims 1-3, 8, 11-14, 16-19, 28, 32-34, 38-43, 52, 53, 58-60, 65, 71-73 and 75 are in proper condition for allowance and consideration and withdrawal of the pending rejections is requested. If the Examiner believes further discussions with applicant's representative would be beneficial in this case, he is invited to contact the undersigned.

The Commissioner is hereby authorized to charge any deficiencies in fees or to credit any overpayments to counsel's Deposit Account No. 19-2380.

Respectfully submitted,

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MARKED UP COPY OF PARAGRAPHS IN AMENDED SPECIFICATION

Figure 5 shows plots of the relationship between the full-width at half [magnitude] maximum for the Raman spectrum and the energy density of the laser light irradiation for samples heated to different temperatures. The full-width at half [magnitude] maximum shown on the vertical axis is a parameter indicating the ratio (W/W_0) between the width W_0 of the spectrum at a position at half of the Raman spectrum intensity for a monocrystalline silicon wafer and the width W of the spectrum at a position at half of the Raman spectrum intensity which was actually obtained for the sample. W and W_0 are defined as the width of the spectrum at a position of half of the Raman spectrum intensity, as shown in Figure 7. In general, a narrow, sharp Raman spectrum means that the crystallinity is excellent. Consequently, in general the width of the Raman spectrum for monocrystalline silicon is the thinnest and the sharpest. It should be noted that the samples which were used were the same as those for which the data shown in Figure 4 was obtained.

Thus the full-width at half [magnitude] maximum shown in Figure 5 is generally a value of 1 or more. It can further be seen that as the value approaches 1, the construction approaches a monocrystalline construction. As can be seen from Figure 5, it is possible to obtain a crystallinity which approaches that of a monocrystal if the temperature to which the sample is heated during irradiation with laser light is increased. It can further be seen that the effects due to heating the sample become saturated at about 500°C.

In the opinion of the present inventors, a region can be regarded as being monocrystalline if the Raman intensity shown in Figure 4 is 0.8 or more, the full-width at half [magnitude] maximum of the Raman spectrum shown in Figure 5 is 2.0 or less, and there are effectively no crystal grain boundaries within the region.

Figure 5 shows the relationship between the energy density of laser light irradiation and the full-width at half [magnitude] maximum of the Raman spectrum for cases in which the temperature to which the sample is heated varies.

MARKED UP COPY OF AMENDED CLAIMS

1. (Amended) An active matrix type display device comprising:

at least two transistors provided on an insulating surface in a XY-branching circuit of a peripheral circuit of said active matrix type display device;

a common gate wiring provided on said insulating surface and connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring provided on said insulating surface and connected with said at least two transistors at one of source and drain of each of said at least two transistors;

a common drain wiring provided on said insulating surface and connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively.

2. (Amended) An active matrix type display device comprising:

at least two transistors provided on an insulating surface in a decoder circuit of a driver circuit of said active matrix type display device;

a common gate wiring provided on said insulating surface and connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring provided on said insulating surface and connected with said at least two transistors at one of source and drain of each of said at least two transistors; and

a common drain wiring provided on said insulating surface and connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively.

3. (Amended) An active matrix type display device comprising:

at least two transistors provided on an insulating surface in a buffer circuit of a driver circuit of said active matrix type display device;

a common gate wiring provided on said insulating surface and connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring provided on said insulating surface and connected with said at least two transistors at one of source and drain of each of said at least two transistors; and

a common drain wiring provided on said insulating surface and connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively.

8. (Amended) An active matrix type display device comprising:

at least two transistors provided on an insulating surface in a driver circuit of said active matrix type display device;

a common gate wiring provided on said insulating surface and connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring provided on said insulating surface and connected with said at least two transistors at one of source and drain of each of said at least two transistors; and

a common drain wiring provided on said insulating surface and connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said at least two transistors, and wherein channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively.